REMARKS/ARGUMENTS

This is in response to the non-final Office Action dated November 1, 2005. Claims 1, 2, 10, and 12 have been amended. No new matter is being presented, and approval and entry are respectfully requested.

REJECTION UNDER 35 U.S.C. § 102

Claims 2, 3, 10, and 12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tsujimoto (U.S. Patent No. 5,345,476). In view of the amendment set forth above and the following remarks, the anticipation rejection is respectfully traversed.

By way of review, Tsujimoto relates to an interference canceller with feedforward transversal filter having switched tap-gain coefficients. The interference canceller is illustrated in FIG. 2. An intermediate frequency signal is applied to a feedforward transversal filter 12 as a signal containing a desired signal $S_n$ and an interference signal $J_n$. See col. 3, ln. 39-42. Feedforward filter 12 produces an output signal S' + J'. See col. 4, ln. 19-38. A subtractor 13 then receives the output signal and the negative input of the subtractor 13 receives an interference estimate J. Id. A feedback transversal filter is connected to the output of decision circuit 15 to compensate for postcursor distortion by supplying an error signal $S_e$ to the subtractor 14. Id. A second feedback filter, or replica filter 18, is connected to the output of the decision circuit 15 for nonlinearly filtering the recovered output signal to produce an estimate S'' of the desired signal S'. See col. 4, ln. 39-44. The estimate S'' is subtracted by subtractor 19 from the output signal S' + J' of the feedforward filter 12 to provide the interference estimate J'' to subtractor 13 when the gate circuit 20 is closed. Id. In the presence of an interference from an undesired source, the interference detector 21 produces a gate signal, causing gate circuit 44 to establish a circuit between subtractors 19 and 13 and gate circuit 44 to nullify the outputs of complex multipliers $41_1$ and $41_2$. See col. 5, ln. 37-41.

Claim 2, as amended, recites a "decision feedback equalizer (DFE) . . . wherein the second adder, the decision device, and the N-tap filter constitute a second continuous feedback loop . . . and the output of the decision feedback equalizer is common with an input of the

decision device." Tsujimoto fails to teach the use of a second *continuous* feedback loop (emphasis added). As shown in FIG. 2, the interference canceller of Tsujimoto includes a gate circuit 20. In the presence of an interference from an undesired signal source, the gate circuit establishes a circuit between subtractors 19 and 13 and gate circuit 44. Thus the second feedback loop of Tsujimoto is not continuous. Moreover, as the Examiner noted in the Office Action dated November 1, 2005, Lim does not disclose "wherein the output of the decision feedback equalizer is common with an input of the decision device."

Independent claims 10 and 12 have been amended to reflect the subject matter of claim 2. Accordingly, it is respectfully submitted that claims 2, 3, 10, and 12 are not anticipated by Tsujimoto nor rendered obvious by Tsujimoto in view of Lim. Reconsideration and withdrawal of the outstanding anticipation rejection are respectfully requested.

REJECTION UNDER 35 U.S.C. § 103

Claims 1, 4, and 11 stand rejected under 35 U.S.C. § 103(a) as obvious over Lim (U.S. Patent No. 5,748,674) in view of Tsujimoto. In view of the amendment set forth above and the following remarks, the outstanding obviousness rejections are respectfully traversed.

By way of review, Lim relates to a decision-feedback equalizer for a digital communication system. The decision feedback equalizer is illustrated in FIG. 6. The decision feedback equalizer includes a feedforward filter 10, a subtractor 20, a slicer 30, a first feedback filter 50, a second feedback filter 60, and an adder 70. See col. 4, ln. 23-38. When a digital signal is outputted from the transmission terminal is received, the feedforward filter 10 filters a pre-cursor ISI signal. See col. 4, ln. 53-57. The first feedback filter 50 receives a predetermined symbol outputted from the slicer 30 and outputs a post-cursor ISI signal with a pipelining delay. See col. 4, ln. 58-64. The second feedback filter 60 also receives the predetermined symbol and outputs a post-cursor ISI signal within the predetermined pipelining delay outputted from the first feedback filter 50. Id.

Claim 1, as amended, recites "first and second feedback equalizer signals . . . wherein the second feedback equalizer signal is continuously supplied as output from a second feedback loop

. . . and wherein the output of the decision feedback equalizer is common with an input of the decision device." As the Examiner noted in the Office Action dated November 1, 2005, Lim does not disclose "wherein the output of the decision feedback equalizer is common with an input of the decision device." Moreover, as discussed above with relation to claim 2, Tsujimoto fails to disclose "first and second feedback equalizer signals . . . wherein the second feedback equalizer signal is continuously supplied as output from a second feedback loop."

Claims 4 and 11 are allowable by virtue of their dependencies for the reasons stated above with regard to claim 2. Accordingly, it is respectfully submitted that claims 1, 4, and 11 are not rendered obvious by Tsujimoto in view of Lim. Reconsideration and withdrawal of the outstanding obviousness rejection as applied to claims 1, 4 and 11 are respectfully requested.

CONCLUSION

While we believe that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner telephone the undersigned attorney in order to expeditiously resolve any outstanding issues.

In the event that the fees submitted prove to be insufficient in connection with the filing of this paper, please charge our Deposit Account Number 50-0578 and please credit any excess fees to such Deposit Account.

Respectfully submitted,
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